IN THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (Currently Amended) A method for forming a semiconductor device, comprising the steps of:

a) forming an insulation layer in a capacitor region and a metal interconnection region on a substrate;

b) forming a first metal interconnection at the metal interconnection region of the insulation layer by performing a dual damascene process;

c) forming a capacitor in the same layer as the metal interconnection in the insulation layer of the capacitor region; and

d) forming a barrier layer and a second metal interconnection on the capacitor and the first metal interconnection in sequence.

2. (Previously Presented) The method as recited in claim 1, wherein the steps b) and c) includes the steps of:

c-1) forming a first trench at the capacitor region of the insulation layer;

c-2) forming the first metal interconnection inside the first trench;

c-3) forming a second trench by removing the insulation layer between the first metal interconnection; and

c-4) forming a capacitor composed of a first electrode, a dielectric layer and a second electrode on the side and the bottom surfaces of the second trench.

3. (Currently Amended) The method as recited in claim 1, wherein the steps b) and c) includes the steps of:

c-5) forming a first trench in the capacitor region of the insulation layer;

c-6) forming a first barrier metal and the first metal interconnection inside the first trench;

c-7) forming a second trench by removing the insulation layer around the first barrier metal;

c-8) forming a third trench in the first barrier metal by removing the first metal interconnection; and

c-9) forming a capacitor ~~composed of~~ having a first electrode, a dielectric layer and a second electrode on the side and the bottom surfaces of the second and the third trenches.

4. (Canceled)

5. (Original) The method as recited in claim 2, wherein the first metal interconnection is of copper.

6. (Original) The method as recited in claim 2, wherein the first and the second electrodes are of a metal selected from a group of Pt, Ru, Ir and W.

7. (Original) The method as recited in claim 2, wherein the dielectric layer is of an oxide selected from a group of Ta oxide, Ba-Sr-Ti oxide, Zr oxide, Hf oxide, Pb-Zn-Ti oxide, Sr-Bi-Ta oxide, and a combination thereof.

8. (Previously Presented) A method for fabricating a semiconductor device, comprising the steps of:

a) forming an insulation layer including a first and a second insulation layers in the capacitor region and the metal interconnection region on a substrate formed with a lower conductive layer;

b) forming an interconnection trench in the metal insulation region, a first trench in the capacitor region and a via hole connected to the lower conductive layer by selectively etching the insulation layer;

c) forming a copper interconnection, a first copper interconnection and a via contact plug by forming a first copper layer in the interconnection trench, the via hole and the first trench and planarizing them;

d) forming a second trench by selectively forming the second insulation layer of the capacitor region;

e) forming a capacitor composed of a first electrode, a dielectric layer and a second electrode on the side and the bottom surfaces of the second trench; and

f) forming a barrier layer on the capacitor and a second copper interconnection on the barrier layer before planarizing the second copper internconnection.

9. (Original) The method as recited in claim 8, wherein the insulation layer includes an etching blocking layer between the first insulation layer and the second insulation layer.

10. (Original) The method as recited in claim 8, further including a hard mask on the second insulation layer.

11. (Original) The method as recited in claim 8, wherein the step of b) forming an interconnection trench, a via hole and a first trench by selectively etching the insulation layer forms the interconnection trench and the first trench simultaneously first, and then forming the via hole.

12. (Original) The method as recited in claim 8, wherein the step of b) forming an interconnection trench, a via hole and a first trench by selectively etching the insulation layer forms the via hole first, and then forming the interconnection trench and the first trench simultaneously.

13. (Original) The method as recited in claim 8, wherein the first and the second copper conductive layers use a reflow method after forming a layer in a sputtering method, a CVD method or an electroplating method.

14. (Original) The method as recited in claim 8, wherein in case of using the electroplating method, a seed layer is formed in a method selected from a group of a physical vapor deposition (PVD), a chemical vapor deposition (CVD) and an electroless deposition, or a combination thereof.

15. (Previously Presented) The method as recited in claim 8, further including the steps of:

g) forming a first barrier metal prior to the first copper layer.

16. (Original) A method for fabricating a semiconductor device, comprising the steps of:

a) forming an insulation layer including a first and a second insulation layers in the metal interconnection region and the capacitor region on the substrate formed with a lower conductive layer;

b) forming an interconnection trench in the metal interconnection region, a first trench in the capacitor region and a via hole by selectively etching the insulation layer;

c) forming a copper interconnection, a via contact plug and a first copper interconnection by forming a first barrier metal and a first copper layer in the interconnection trench, the via hole and the first trench and planarizing them;

d) forming a second trench by selectively etching the second insulation layer around the first copper interconnection in the capacitor region;

e) forming a third trench in the first barrier metal by selectively etching the first copper interconnection;

f) forming a capacitor composed of a first electrode, a dielectric layer and a second electrode on the side and the bottom surfaces of the second and the third trenches; and

g) forming a second copper interconnection by forming a second copper layer on the capacitor and planarizing it.

17. (Original) The method as recited in claim 16, wherein a second barrier metal is formed prior to the formation of the second copper layer.

18. (Original) The method as recited in claim 16, wherein the first and the second barrier metals is of one selected from a group of Ta, TaN, TiN, WN, TaC, WC, TiSiN and TaSiN, and a combination thereof.